Verification Methodology For A Complex System On A Chip

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Verification methodology plays an important role in the functional verification of RTL design of the communication based SOC and yields the complete code coverage. Following the test Plan, the test...

ADVANCED VERIFICATION METHODOLOGY OR COMPLEX SYSTEM CHIP ...

A. Higashi et al.: Verification Methodology for a Complex System-on-a-Chip Register-Transfer Level (RTL), where logic circuits are described using a Hardware Description Language (HDL). We have now established a new design meth- odology for SOCs. At the beginning of SOC design, we introduce a system-level simulation technique.

Verification Methodology for a Complex System-on-a-Chip

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Verification Methodology for a Complex System-on-a-Chip

Verification Methodology for a Complex System-on-a-Chip VAkihiro Higashi VKazuhide Tamaki VTakayuki Sasaki (Manuscript received December 1, 1999) Semiconductor technology has progressed to the point where it is now possible to implement system-level functions on a single LSI chip. However, traditional LSI verifi-Verification Methodology for a Complex System-on-a-Chip

Verification Methodology For A Complex System On A Chip

Verification Methodology for a Complex System-on-a-Chip Assertion-based verification (ABV) affirmed as an effective methodology for functional verification, i.e., design specification conformance, of embedded systems. Verification Methodology for a Complex System-on-a-Chip Advanced Verification Methodology for Complex System on Chip Verification. A

Verification Methodology For A Complex System On A Chip

This is a guest post by S3 Group that provides design, verification and implementation of the most complex IC solutions. This paper describes the design & verification methodology used on a recent large mixed signal System on a Chip (SoCs) which contained radio frequency (RF), analog, mixed-signal and digital blocks on one chip.

Mixed Signal Design & Verification Methodology for Complex ...

al.: Verification Methodology for a Complex System-on-a-Chip Register-Transfer Level (RTL), where logic circuits are described using a Hardware Description Language (HDL). We have now established a new design meth-odology for SOCs. At the beginning of SOC design, we introduce a system-level simulation technique. Verification Methodology for a Complex

Verification Methodology For A Complex System On A Chip

This paper presents a novel and alternative methodology of logic or functional verification of a system-on-a-chip integrated- circuit. This methodology was used by our company for a successful and timely tape-out of our SoC. We will show a complete verification methodology that resulted in a fully- functional first sil

A Methodology for Timely Verification of a Complex SoC/CHIP

Mixed Signal Design & Verification Methodology for Complex SoCs 8 The digital and analog sections interact by sharing data and controlling each other's events. This allows for event-driven analog blocks. Verilog can be extended to support real value nets (wreal), discussed further in Section 3.5.1. 3.3 Design Flow

Mixed Signal Design & Verification Methodology for Complex ...

Verification of integrated L1 HW, SW and protocol stack In a conventional design and developmental flow, the verification of L1 SW, which would be typically executed in embedded environment, is done once the HW prototype is available. This increases the development cycle time for complex wireless systems. Recently, advances have been

A SystemC-based Verification Methodology for Complex ...

"A hierarchical analysis and verification methodology for complex VLSI systems." (1988).Electronic Theses and Dissertations.Paper 637. Title: A hierarchical analysis and verification methodology for complex VLSI systems. Created Date:

A hierarchical analysis and verification methodology for ...

KEYWORDS Advanced verification Methodology, Verification Simulation software, Test Bench. 1. INTRODUCTION The complexity of the chip has increased in present years and integration of more numbers of components in a single Soc makes verification of any Soc design very critical. We need proper verification methodology for any Soc or IP.

advanced verification methodology for complex system on ...

A SystemC-Based Verification Methodology for Complex Wireless Software IP. Previous Chapter Next Chapter. ABSTRACT. The implementation of a complex hardware Intellectual Property (IP) together with complex lower-level software and the integration into a system platform poses tough challenges to the design and verification engineers ...

A SystemC-Based Verification Methodology for Complex ...

Home Conferences DAC Proceedings DAC '01 A new verification methodology for complex pipeline behavior. ARTICLE . A new verification methodology for complex pipeline behavior. Share on. Authors: Kazuyoshi Kohno. Toshiba Corporation Semiconductor Company, 580-1, Horikawa-Cho, Saiwai-Ku, Kawasaki, 212-8520, Japan .

A new verification methodology for complex pipeline ...

For complex assemblies, the verification of design and the associated production methods is currently fragmented, prolonged and sub-optimal, as it uses digital and physical verification stages that are deployed in a sequential manner using multiple systems.

Early design verification of complex assembly variability ...

For complex assemblies, the verification of the design intent and the associated production methods is currently fragmented, prolonged and sub-optimal, as it is based on the sequential consideration of various aspects in the digital and physical domains using a range of systems.

Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

Three-Dimensional Integrated Circuits (3DICs) have recently attracted great interest from researchers and IC designers as a possible solution to fill the gap between device and interconnect scaling. Various studies have demonstrated the potential performance improvement of 3DICs by eliminating long interconnects, repeaters, and clock buffers.

One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

Despite its increasing importance, the verification and validation of the human-machine interface is perhaps the most overlooked aspect of system development. Although much has been written about the design and developmentprocess, very little organized information is available on how to verifyand validate highly complex and highly coupled dynamic systems. Inability toevaluate such systems adequately may become the limiting factor in our ability to employ systems that our technology and knowledge allow us to design. This volume, based on a NATO Advanced Science Institute held in 1992, is designed to provide guidance for the verification and validation of all highly complex and coupled systems. Air traffic control isused an an example to ensure that the theory is described in terms that will allow its implementation, but the results can be applied to all complex and coupled systems. The volume presents the knowledge and theory ina format that will allow readers from a wide variety of backgrounds to apply it to the systems for which they are responsible. The emphasis is on domains where significant advances have been made in the methods of identifying potential problems and in new testing methods and tools. Also emphasized are techniques to identify the assumptions on which a system is built and to spot their weaknesses.

Three-Dimensional Integrated Circuits (3DICs) have recently attracted great interest from researchers and IC designers as a possible solution to fill the gap between device and interconnect scaling. Various studies have demonstrated the potential performance improvement of 3DICs by eliminating long interconnects, repeaters, and clock buffers. Though 3DICs are attractive, there are significant challenges associated with this topic. The most fundamental issue in 3DIC is heat dissipation. The thermal effect has impacted the conventional high-performance 2DICs in deep sub-micron technology nodes. Its effect will aggravate 3DICs due to two major reasons: higher power density, and lower thermal conductivity caused by more insulating dielectric layers. Furthermore, while 3D integration provides more design flexibility, this technology also introduces much higher design complexity. The existing 2D physical design methodology cannot be simply extended to a 3D case because of the huge obstacles in the z-direction and thermal constraints. Efficient design flows and algorithms must be developed to facilitate 3DIC design. This dissertation proposes a design and verification methodology, along with analyses of delay, thermal, and reliability of a 3D system. The methodology uses commercial 2D CAD tools with Python and Tcl scripts to link them together. The scripts modify the output files (or databases) of the commercial tools and add 3D features to them. The entire flow achieves RTL-to-GDSII physical design automation for 3DICs. Design trade-offs and timing reliability of 3D systems are two other major issues of this dissertation. Non-idealities threaten to diminish the benefit and may cause reliability problems in 3D systems. These non-idealities must be monitored during the design procedure. With a fast yet accurate temperature dependency model, these non-idealities were successfully taken into consideration during both design and verification phases. The final performance analy.

This book brings together a selection of the best papers from the fifteenth edition of the Forum on specification and Design Languages Conference (FDL), which was held in September 2012 at Vienna University of Technology, Vienna, Austria. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems.

This four-volume set (CCIS 643, 644, 645, 646) constitutes the refereed proceedings of the 16th Asia Simulation Conference and the First Autumn Simulation Multi-Conference, AsiaSim / SCS AutumnSim 2016, held in Beijing, China, in October 2016. The 265 revised full papers presented were carefully reviewed and selected from 651 submissions. The papers in this first volume of the set are organized in topical sections on modeling and simulation theory and methodology; model engineering for system of systems; high performance computing and simulation; modeling and simulation for smart city.

System-On-a-Chip Verification: Methodology and Techniques is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign- off. The topics covered include Introduction to the SOC design and verification aspects, System level verification in brief, Block level verification, Analog/mixed signal simulation, Simulation, HW/SW Co-verification, Static netlist verification, Physical verification, and Design sign-off in brief. All the verification aspects are illustrated with a single reference design for Bluetooth application. System-On-a-Chip Verification: Methodology and Techniques takes a systematic approach that covers the following aspects of verification strategy in each chapter: Explanation of the objective involved in performing verification after a given design step; Features of options available; When to use a particular option; How to select an option; and Limitations of the option. This exciting new book will be of interest to all designers and test professionals.

Verification is increasingly complex, and SystemVerilog is one of the languages that the verification community is turning to. However, no language by itself can guarantee success without proper techniques. Object-oriented programming (OOP), with its focus on managing complexity, is ideally suited to this task. With this handbook—the first to focus on applying OOP to SystemVerilog—we'll show how to manage complexity by using layers of abstraction and base classes. By adapting these techniques, you will write more "reasonable" code, and build efficient and reusable verification components. Both a learning tool and a reference, this handbook contains hundreds of real-world code snippets and three professional verification-system examples. You can copy and paste from these examples, which are all based on an open-source, vendor-neutral framework (with code freely available at www.trusster.com). Learn about OOP techniques such as these: Creating classes—code interfaces, factory functions, reuse Connecting classes—pointers, inheritance, channels Using "correct by construction"—strong typing, base classes Packaging it up—singletons, static methods, packages